Crystalline Si Photovoltaics

Arthur Weeber
Outline

• Short introduction ECN
• Introduction ECN Solar Energy
• General Si solar cells
• Crystalline Si Photovoltaics
  - Feedstock
  - Wafering
  - Cell processing
  - Module technology
  - Costs and environmental
• Summary
Petten: ECN; NRG; JRC; TYCO
Targets ECN research

Transition to renewable energy supply:

- efficiency improvement
- development of renewable energy
- clean use of fossil fuels

maximum reliability
minimum environmental burden
optimal cost effectiveness
ECN Programme units

Strategically
Policy Studies

Energy savings
Energy Efficiency in Industry
Renewable Energy in the Built Environment

Renewable energy
Solar Energy
Wind Energy
Biomass, Coal & Environmental research

Clean use fossil fuels
Hydrogen & Clean fossil fuels

Support
Engineering & Services
ECN Solar Energy
Solar Energy

• Silicon Photovoltaics
• Thin-Film Photovoltaics
• PV Module Technology

Objective:
• Price of solar electricity in 2015 the same as consumer electricity price, and after that even lower
  - High efficiency
  - Reduction of material use
  - Cost effective and environmental friendly processes and products
  - Long lifetime of the modules
PV technology development: no revolution, but evolution

- tf-Si = thin-film silicon
- CIGSS = copper-indium/gallium-selenium/sulfur
- c-Si = wafer-type crystalline silicon
- OSC = organic solar cells
- new concepts = advanced versions of existing technologies & new conversion principles

(free after W. Hoffmann)
Thin-film photovoltaics

- Sensitised oxides
  - efficiency, stability, manufacturing technology
  - solid state version: in 2015 $\eta=8\%$ for 10x10 cm$^2$
device with >10 year outdoor stability
ECN Solar Energy

Thin-film photovoltaics
- Organic solar cells
  - device fabrication, efficiency and stability
  - in 2015 $\eta=8\%$ for 10x10 cm$^2$ device
  - with >10 year outdoor stability

Collaboration of ECN, TNO
ECN Solar Energy

Thin-film photovoltaics

- Thin-film silicon
  - R-2-R deposition of (n,i,p) silicon on foils
  - Development of thin-film Si tandems
  - In 2015 a 0.3x1 m^2 PV module $\eta=12\%$ at 0.8€/Wp
New concepts
- Improved spectrum utilization
- Flat plate concentrator

UV visible infrared

Solar spectrum (Air Mass 1.5; 1000 W/m²)

Available for conversion in crystalline Si

1100 nm ~ 1.1 eV = Si bandgap
ECN Solar Energy

**PV systems**
- grid interaction
- system design & monitoring
- standards and guidelines
Crystalline Si PV technology

Objective:
- Price of solar electricity in 2015 the same as consumer electricity price, and after that even lower
  - High efficiency
    - 18% module efficiency for crystalline Si PV
  - Reduction of material usage
    - Thin wafers (<150 µm compared to current >240 µm)
  - Cost effective and environmental friendly processes and products
  - Long lifetime of the modules (>30 yr for crystalline Si)
  - Energy Pay Back Time < 1 yr
Cell structure

Crystalline silicon solar cell (minority carrier device)

- Base: B doped Si (p-type)
- Emitter: P doped layer (n-type)
  - Recombination losses in base and emitter
  - Voltage over pn junction

- Metallization for contacts
  - Shading losses
  - Resistance losses

- Antireflection coating to enhance current

- Surfaces: recombination losses
Cell structure

Crystalline silicon solar cell

- Base: B doped Si (p-type)
- Emitter: P doped layer (n-type)
  - Voltage over pn junction
  - Recombination losses

- BSF: p⁺ doped layer
  - Highly doped
  - Reduced recombination
Cell structure

Losses in crystalline silicon solar cell

- Colour mismatch
- Fundamental recombination \[ \eta \leq 30\% \]
- Additional recombination
  - Impurities, defects, surfaces
- Shading
- Reflection, absorption and transmission
  - Absorption at the rear
- Resistance
- Non-ideal band gap

Crystalline Si solar cell: \( \eta = 13\text{-}20\% \)
Cell characterization

- Current Voltage (IV curve)
  - Open circuit voltage $V_{oc}$
  - Short circuit current $J_{sc}$
  - Efficiency
  - Resistance losses
Cell characterization

- Internal Quantum Efficiency IQE
  - IQE = collected carriers / absorbed photons
- Depth profile cell quality

![Graph showing IQE (%)](image)
Crystalline Si PV technology

- Feedstock
  - Effect impurities on cell output
- Wafers
  - Monocrystalline Si
  - Multicrystalline Si
- Cell technology
  - High efficiency with industrial in-line processing
- Module Technology
  - Module design integrated with cell concept
  - Simple interconnection and encapsulation
- Costs and environmental aspects
Crystalline Si PV technology

• Feedstock
  - Effect impurities on cell output
• Wafers
  - Monocrystalline Si
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• Cell technology
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• Module Technology
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• Costs and environmental aspects
Feedstock production

quartz, carbon

existing; 900,000 ton/y

mg-Si

under development, virtually unlimited

under development, virtually unlimited

refining (silanes)

existing; 26,000 ton/y

eg-Si

under development high cost

semiconductor industry

solar grade Si

demand
13,000 ton (2004)
~200,000 ton (2020)

semi-prime
4500 ton/y

off-grade
2000 ton/y
Feedstock production

• Direct route: SOLSILC process

• plasma furnace: SiC from pure SiO₂ and pure C pellets of SiC and SiO₂ → Si(L)
Feedstock: ingot growth

- Multicrystalline Si ingot growth
Feedstock: effect impurities

- Feedstock
  - Melting
  - Crystallization
- Ingot
  - Sawing
- Wafer

Decreasing:
- $[O_i]$

Increasing:
- dopant conc.
- metal conc.
- $[C_s]$
Feedstock: effect impurities

- Feedstock
- Ingot
- Wafer

Impurities:
- Fe
- Ti
- Al (tentative)

Graph showing ppmw concentration for each impurity in feedstock, ingot, and wafer.
Feedstock: effect impurities

Impurities added to feedstock

Effect Ti and O on cell output clearly visible
Feedstock: effect impurities

Impurities added to feedstock
- Ingot growth
- Wafering
- Cell processing
- Characterization
- Model development
  - $1/L_{\text{eff}} \propto 1/\tau \propto C_{\text{imp}}$
  - Segregation during growth
  - Solar cell modeling

- Needed to define Solar Grade Si

![Graph showing cell efficiency vs. impurity concentration](graph.png)

- 14.5% cell techn.
- 17% cell techn.

Our results: 5 ppmw Al or 10 ppmw Ti

High efficiency reduction

Relative to high-purity feedstock
Wafer technologies

Pulling of Single Crystals (Czochralski)

Casting of Silicon Blocks

Bridgman Solidification

Heat Exchange Method

Edge defined Film fed Growth

Ribbon Growth on Substrate
Wafer technologies

- Multicrystalline Si ingot growth
Wafer technologies

• From ingot to mc-Si wafer
Wafer technologies

• High quality monocrystalline Si material
  - Low impurity concentration
  - Low defect concentration
  - Higher efficiency (15-17% in industry, 20% pilot)
  - Higher costs per cell

• Lower quality multicrystalline Si material (mc-Si)
  - Higher impurity concentration
  - More defects
  - Lower efficiency (13-15% in industry, >16% pilot)
  - Lower costs per cell

• For both technologies: high sawing losses (about 50%)!
Wafer technologies

• Ribbon technologies (multicrystalline Si)

• Substrate growing and crystallization in the same direction

Edge defined Film-fed Growth (SCHOTT Solar)

String Ribbon
Wafer technologies

• ECN’s ribbon technology
  Ribbon Growth on Substrate
  RGS

• Substrate growing perpendicular to crystallization
Wafer technologies

Ribbons:
- Better use of Si material (about factor 2)
- Lower initial material quality
- Lower efficiencies

- EFG/SR: about 14% (industry)
- RGS: about 13% (lab)
  - Very high throughput

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<table>
<thead>
<tr>
<th>Material</th>
<th>Pull Speed [cm/min]</th>
<th>Throughput [cm²/min]</th>
<th>Furnaces per 100 MW</th>
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<tbody>
<tr>
<td>EFG</td>
<td>1.7</td>
<td>165</td>
<td>100</td>
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<tr>
<td>SR</td>
<td>1-2</td>
<td>5-16</td>
<td>1175</td>
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<tr>
<td>RGS</td>
<td>600</td>
<td>7500</td>
<td>2-3</td>
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</table>

*[J. Kalejs, E-MRS 2001 Strasbourg]*
Wafer Technology

RGS cell efficiencies using industrial process
- Average efficiency 12.5%.
- Current top efficiency 13% confirmed
- High efficiency lab processing 14.4% confirmed

- ~100 µm thin RGS wafer made
  - Efficiency around 11%
  - 2.9 g Si/Wp (nowadays ~10 g Si/Wp)
Cell processing

- Saw damage removal
  - Texturing for enhanced light coupling (better efficiencies)
- Emitter diffusion
  - Material improvement by gettering
- SiN$_x$ deposition as antireflection layer
  - Material improvement by passivation
  - Reduced surface recombination (surface passivation)
- Metallization
  - Ag front side
  - Al rear side (so-called Back Surface Field)
- Sintering for contact formation
Cell processing

**Batch processing**
- Wafers in carriers
- Each process step well controlled
- Used for high efficiency processing

**Diagram:**
- etching
- junction
- ARC
- contacts
- load
- transport
- unload
Cell processing

ECN's inline processing
Horizontal wafer transport on belts (wafer in; cell out)
- No wafer carriers
- Large and thin wafers easier to handle (cost reduction)
Cell processing

**Examples from industry**
Batch processing BP Solar

In-line processing SCHOTT Solar
Cell processing

ECN Baseline process
- Multicrystalline p-type Si
- Acidic texturing / saw damage removal
- P diffusion using belt furnace
- Deposition of SiN$_x$
- Metallization (Ag front, full Al rear)
- Simultaneous sintering both contacts

Results
Processing complete columns of wafers during two years
- Average 16%
- In industry about 15%
Texturing

Acidic texturing of mc-Si

Alkaline and acidic etch
Texturing

Acidic texturing of mc-Si
Texturing

Acidic texturing of mc-Si

- Lower reflection, higher efficiency
  - About 0.5% absolute
- Better appearance
Texturing

Surface structure texturing Si

- **Monocrystalline Si**
  - Alkaline etching (NaOH or KOH)
  - Anisotropic etching
    - (111) planes slowest etching rate
    - Pyramids on (100) substrates

- **Multicrystalline Si**
  - HF/HNO₃ etching
  - Isotropic etching
    - Random structure
Texturing

Alkaline etching of Si

\[ \text{Si} + \text{OH}^- + \text{H}_2\text{O} \rightarrow \text{SiO}_3^{2-} + \text{H}_2\text{gas} \]

- Higher concentrations and higher \( T \)
  - Almost isotropic etching
  - High etching rate
  - Used to remove saw damage (5-10 \( \mu \text{m} \))
  - High reflectance (~30%)
Texturing

Alkaline etching of Si

- Lower concentrations and lower $T$
  - Anisotropic etching
    - (111) planes slowest etching rate
    - Pyramids as texture on (100) substrates
    - Low reflectance (~10%)
  - But, low etching rate
Texturing

Acidic etching of Si

Mixture HF/HNO₃

Oxidation

\[ 3 \text{Si} + 4 \text{HNO}_3 \rightarrow 3 \text{SiO}_2 + 4 \text{NO}_{\text{gas}} + 2 \text{H}_2\text{O} \]

Oxide removal

\[ \text{SiO}_2 + 4 \text{HF} \rightarrow \text{SiF}_4_{\text{gas}} + 2 \text{H}_2\text{O} \]

- Obtained surface morphology depends on composition
  - Polishing
  - Defect etching
  - Texturing
Emitter processing

Needed to form p-n junction

- Apply P source
- Diffusion at ~900 C for about 10 minutes

- Depth about 0.5 µm
- P concentration at surface: > $2 \times 10^{20}$ cm$^{-3}$
  - Higher concentration needed for good contacting
  - However, it will result in additional recombination losses

Improved emitter/front side processing can give an efficiency gain of more than 0.5% absolute
Emitter processing

Effect dopant concentration on IQE

- Improved blue response (up to 550 nm) for lower dopant concentration
- Higher $V_{oc}$ and higher $J_{sc}$: higher efficiency!

![Graph showing the effect of dopant concentration on IQE and the impact of diffusion barrier thickness on IQE.](image)
Emitter processing

Additional effect of emitter processing

• So-called gettering
  - Diffusion of impurities to P rich layers (P-gettering)
  - Impurities will not affect efficiency in those P rich layers

• Improved bulk quality and, thus, higher efficiency
SiN$_x$ deposition

Applied using chemical vapour deposition
- Low pressure chemical vapour deposition (only surface passivation, ~700 C)
- Plasma enhanced chemical vapour deposition (different systems, ~400 C, 0.5-10 nm/s)
- Sputtering (several nm/s)

Functions SiN$_x$:H layer
- Antireflection coating (70-80 nm)
- Surface passivation (reduced recombination at the surface)
- Bulk passivation (improved material quality)
  - During anneal H diffuses into bulk and makes defects/impurities electrically inactive
**SiN_x deposition**

Plasma Enhanced Chemical Vapour Deposition (PECVD)

- Parallel plate system
  - Direct plasma
    - Wafers as electrodes
    - Ion bombardment dependent on plasma frequency
    - Damaged layer

- Remote PECVD
  - No ion bombardment

Aberle et al.
SiN$_x$ deposition

ECN MicroWave Remote PECVD

- Deposition rate about 1 nm/s
SiN\textsubscript{x} deposition

Expanding Thermal Plasma (ETP)
- Developed by TU/e
- Deposition rate 5-10 nm/s
- TU Delft: for thin film Si depositions
SiN$_x$ deposition

Optical specifications SiN$_x$;H layer

- Refractive index: $n=2.1$
  higher $n$ causes absorption at lower wavelength

$$n_1 = \sqrt{n_0 n_2} \quad \quad d_1 = \frac{\lambda_0}{4 n_1}$$

- Ideal for air-Si: $n=1.9$; $d=\sim 80$ nm
- Ideal for air-glass-Si: $n=2.3$; $d=\sim 65$ nm
  (absorption SiN$_x$ too high)

- $n$ can be tuned with gas composition
- Higher $n$: more Si (SiH$_4$)
- Lower $n$: more N (NH$_3$)
SiN$_x$ deposition

Optical specifications SiN$_x$:H layer

- Different layer thickness: different colour
Gettering and bulk passivation (emitter and SiNₓ:H)

Improved bulk quality using gettering and passivation

- Lifetime > 100 µs will hardly affect cell efficiency (diffusion length 2 times cell thickness)
- Besides higher efficiency, gettering and passivation will result in a narrower efficiency distribution.
Metallization

Screen-printing process and sintering in belt furnace
Metallization

Principle screen-printing process

- Metallization paste is ‘pressed’ through pattern in screen
- Paste contains metal particles and oxides (etches Si at higher T)
Metallization

Ag front side metallization
• Fine line metallization printed through patterned screen
**Metallization**

Fine line printing
- Reduced shading losses
- Contact resistance might be critical
Metallization

• Other techniques:

• Plating (electroless)

• Dispensing

• Pad printing

• Roller printing
Metallization

Al rear side (Back Surface Field to reduce recombination at surface)

- After sintering step (around 800 C, few seconds) highly doped layer
- Better BSF when thicker and higher doped
Efficiency ECN process

Results ECN Baseline process
Processing two complete columns (different ingots) of wafers during 2 years
• Average 16.0%
• In industry about 15%

Wafer size: 125x125 mm²
Thickness: ~300 µm
Material: p-type mc-Si
Efficiency ECN process

- High-efficiency (17%) **in-line** process (300 µm thick; 156 cm² mc-Si)
  - 50 cells processed (best efficiency 17.1%; average 16.8%)
  - Module made using cover glass with ARC
    Full area efficiency 14.8%; encapsulated cell eff: 16.8%

\[
V_{OC}=22.2 \, V; \quad I_{SC}=5.76\, A; \quad FF=0.738; \quad P=94.3 \, Wp
\]
Efficiency ECN process

- From 2000 up to now

---

**Efficiency ECN process**

- From 2000 up to now

---

**Efficiency (%)**

- initial (<2000): 12.5
- lifetime: 13.7
- BSF: 14.9
- front side passivation and emitter: 16
- light management: 17

**ECN 2005**

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**IQE (%)**

- front side and emitter
- bulk and rear side
- rear side reflection

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**wavelength (nm)**

- 300 to 1100

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**Energy research Centre of the Netherlands**

www.ecn.nl
Future improvements

Thin wafers
• Rear side critical

Minority carrier density
• Combination of generation and recombination
  17.0%: good bulk and rear
  15.9%: good bulk, low rear
  15.7%: low bulk, good rear
  15.3%: low bulk and rear
  14.3%: as 15.9%, but thin
Future improvement

Al rear side (Back Surface Field to reduce recombination at surface)

• 17% reached on 300 µm thick wafers

However:

• Bowing for thinner wafers
• Recombination losses too high for high efficiencies (>18%)
• Internal reflection too low (~70%) for high efficiencies
Future improvements rear side

Thin wafers

- Rear side critical (bowing, reflection, BSF)
- New rear side processing using for example SiN$_x$
  - Higher efficiencies for thinner wafers

SiN$_x$ for rear side passivation
Local rear contacts / BSF

![Graph showing efficiency vs. cell thickness for current and future rear sides](graph.png)
Future improvements rear side

Thin wafers

- New rear side processing using SiN$_x$
  - 16.4% obtained by ECN with baseline-like processing
  - About 1% absolute higher than reference with Al BSF
    (obtained efficiency depends on Si material quality)
Future improvements

Thin wafers (less dependent on material quality)
• Improved light management
  - Texturing
  - Light trapping
• Improved emitter (reduce losses)
• Perfect surface passivation
  - Both surfaces
• Less metallization losses
  - Series resistance (contact and line resistance)
  - Reduced shading losses

20% mc-Si cell efficiency should be possible! (long term)
Other industrial cell concepts

Laser Grooved Buried Contacts
BP Solar
• Monocrystalline

Rear side contacted cell
SunPower
• ~20%!
• High quality and expensive material
Other industrial cell concepts

SunPower
- Cell 21.8%
- n-type material
- Module: full area 18.1%

Sanyo
- HIT cell: 21.8%
- n-type material
- Emitter deposited
# Record efficiencies

<table>
<thead>
<tr>
<th></th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monocrystalline (4 cm²):</td>
<td>24.7%</td>
</tr>
<tr>
<td>Monocrystalline (149 cm²):</td>
<td>21.5%</td>
</tr>
<tr>
<td>Multicrystalline (1 cm²):</td>
<td>20.3%</td>
</tr>
<tr>
<td>Multicrystalline (137 cm²):</td>
<td>18.1%</td>
</tr>
<tr>
<td>ECN multi (156 cm²):</td>
<td>17.0%</td>
</tr>
</tbody>
</table>

Single layer ARC; homogeneous emitter; inline processing

Highest efficiency with completely inline processing
Module technology

Conventional module technology (soldering)

Glass
EVA
Solar cells
EVA
Tedlar foil

Series connection

Interconnection strips (tabs)
Module technology

Conventional module technology

interconnection

lamination
Module technology

Pilot-line tabber-stringer for interconnection
Module technology

Pilot line to be built at ECN

Fully automated and reliability-tested interconnection process for back-contact cells and suitable for thin and fragile cells
Module technology

New module technology:
• New cell designs needed
  - Back contacted
  - Simple interconnection
  - Can be used for thin cells
Module technology

Emitter Wrap Through:
- No metallization on the front
- Thousands of holes
Module technology

ECN’s PUM concept:
• More energy from attractive cells
• 2-3% less shading
• Resistance losses independent on cell size (only on size unit cell)
• Standard cell processing except:
  - Laser drilling holes
  - Junction isolation around holes

Mother Nature’s water lily
Module technology

ECN’s PUM concept:
• Single shot interconnection and encapsulation

Single step module assembly

Solar cell interconnection with electrically conductive adhesive

- Glass plate
- PUM cell
- Adhesive
- Rear side foil
- Metallisation through hole
- EVA Encapsulant
- Insulating Varnish
- Conductive Adhesive
- Aluminum
- Polyester
- Conductive Adhesive
Module technology

ECN’s PUM process:

• Foil preparation
• Apply conductive adhesive instead of soldering (lower stress)
• Pick and place cells
• One step curing and encapsulation
Module technology

ECN’s PUM result:
• Full size module (71×147 cm²)
• 128 Wp (15.8% encapsulated cell efficiency)
• 0.6-0.8% absolute efficiency gain

Best PUM cell result up to now:
• 16.7% (225 cm²)

At this moment PUM is the only integrated concept for cell and module
PV market

Annual market growth more than 40%

Growth rate 2004: 67%
2005: 1720 MWp (+44%)
Japan: ~50% market share

Photon International, 2006
PV market

More than 90% crystalline Si technology

Photon International, 2006
PV market

Expected market: solar the most important primary energy source

Wissenschaftliche Beirat 2003
Costs PV

Contributes wafer is about 45%!
Thinner wafers, or better ribbons, important!

Price solar electricity:
0.20-0.50 €/kWh
(depending on location)

NL: \(\sim 0.50 \) €/kWh
Cost reduction PV

• Less material use
  • Thin ribbons
  • Less module materials
• High efficiencies for the same process costs
  • Advanced processing
  • New cell design
• Easy manufacturing
  • Automation
  • Easy module manufacturing
• High lifetime
• Improved yearly system output
Cost reduction PV

- Expected costs

Typical turn-key system price (€/Wp)

1000 GWp worldwide
200 GWp in EU (200,000 jobs)
Cost reduction PV

- Expected costs based on learning curves (EU project Photex)
  - Combined effect of technology development, experience, ....
  - Progress ratio PR should be around 80%
Cost reduction PV

- Expected costs

- Solar competitive between 2010-2020

Source: RWE Energie AG and RSS GmbH

Towards an Effective European Industrial Policy for PV.ppt / 05.06.2004 / Rapp

RWE SCHOTT Solar GmbH
Environmental aspects

• Energy Pay Back Time 2005

Energy Pay-Back Time
(grid-connected, roof-top PV system; irradiation 1700 resp. 1000 kWh/m2/yr)
Environmental aspects

Energy Pay Back Time 2005 and 2010

- Low energy consumption especially for Solar Grade Si
- Low material use (abundance)
- High efficiency
- High lifetime modules
- Environmental friendly processes
- Recycling
Conclusions

• Solar Grade Silicon needed for growing market
  - Effect of impurities on cell efficiency should be known
• Less Si use with ribbons
• Improved processing has led to 17% mc-Si efficiency using in-line processing
• New processes for thin wafers/ribbons under development
• Integrated cell and module design like PUM needed
• High module lifetime

Then
• Cost reduction possible
  - Will be competitive with bulk electricity price
• Energy Pay Back Time can be reduced to <1 year
• Solar energy will be the most important primary energy source in 2100
Applications at ECN
Applications
Thank you for your kind attention

Floriade (2.3 MWp PV)

Information / internship
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